Letters

Comments on "On Deembedding of Port Discontinuities in Full-Wave CAD Models of Multiport Circuits"

James C. Rautio

Several additional comments are appropriate for the above well-written paper [1] on electromagnetic (EM) deembedding. The above paper [1] extends the short-open-calibration (SOC) deembedding technique to multiple coupled ports [vector short-open-calibration (VSOC)].

While not widely realized, the SOC technique is closely related to the double-delay EM deembedding first described in [2] and in commercial use in Sonnet for nearly two decades [3], [4]. To our knowledge, [2] is the first paper to apply modern microwave measurement deembedding techniques to EM analysis, initiating EM research in this area.

Double-delay deembedding uses two standards, a through line of length L, and a second line of length $2L$. The SOC technique uses a single through line of length $2L$. This standard is identical to the $2L$ double-delay standard, except that the SOC standard has a third (internal) port midway between the two end ports.

The $2L$-length double-delay deembedding standard is obtained from the SOC standard by short circuiting the third port. The L-length double-delay standard is obtained from the SOC standard by exciting the SOC standard so as to place a perfect electric conductor (PEC) wall at the midpoint of the line [1, Fig. 5(b)] and obtaining the short-circuit admittance of the resulting L length of line. The Y-parameters of the L-length line are then formed from the short-circuit admittance so calculated. Thus, the double-delay data set can be completely obtained from the SOC data set.

Double-delay deembedding requires the port discontinuity to be a pure shunt admittance. The SOC formulation allows any port discontinuity. However, as currently formulated, SOC neither explicitly provides the port connecting line characteristic impedance, nor the naked port discontinuity (the port discontinuity with no connecting transmission line). Thus, the SOC can be applied to a wider range of problems, but the double delay provides more information when the port discontinuity is appropriate. Unification of the double delay and SOC, so that a SOC calibration can determine the characteristic impedance and naked port discontinuity, is currently a topic of our research.

The double-delay restriction to pure shunt admittance port discontinuities is not a limitation, as applied to [3] and [4] for sidewall ports [1, Fig. 2(a)] because the port discontinuity is always a pure shunt admittance. When nonsidewall ports (including internal ports, [1, Fig. 2(b)] and via ports [1, Fig. 2(c)]) are deembedded, a deembedding standard formed from the nonsidewall port, plus a sidewall port and connecting transmission line is used. Deembedding the sidewall port and shifting the reference plane to the nonsidewall port yields the nonsidewall port discontinuity. The completely general nonsidewall port is then deembedded using $ABCD$ matrices in the usual manner.

It is advantageous to use, whenever possible, sidewall ports that have only a pure shunt admittance. In this case, as pointed out in [2], the $ABCD$ matrix for the port discontinuity (with the connecting transmission line removed) has C equal to the port discontinuity admittance, while $A = D = 1$ and $B = 0$. Any difference from these values for A, B, or D indicates a deembedding failure. This provides a self-diagnostic capability for double delay, provided the port discontinuity is a pure shunt admittance. When SOC is applied to shielded analysis, this same check can be used, provided the SOC can be modified to allow determination of the naked port discontinuity.

When using SOC to deembed a general port discontinuity (for example, in an unshielded analysis, where double delay is inappropriate), this self-diagnostic capability is not available. Such self-diagnostic capability is critical in applied design. Finding some way to provide this to the SOC as applied to arbitrary port discontinuities is, in the author's opinion, a high-priority area for future research.

Failure mechanisms for both double delay and SOC include selection of L so short that the port fringing fields interact, multiple propagating modes (including surface waves, as discussed in [1]), and, for shielded analysis, box resonances. Note that some of these failure mechanisms also occur when the analyzed circuit is fabricated and should be viewed as deficient design rather than deembedding failure.

It is stated in [1] that error for VSOC is less than double delay for weakly coupled ports. This is supported by larger differences (in decibels) between VSOC results and Sonnet results for small-magnitude S-parameters in data presented in [1]. We suggest that the differences are not error and that they are not due to the deembedding approach used, rather they are due to the differences between shielded and unshielded analysis. Differences seen when using different values for L can be considered error; however, lacking knowledge of the exact correct answer, we can not determine the magnitude of the error.

The substrate thickness in [1] is small compared to wavelength (8% of a wavelength at 20 GHz) so higher order microstrip modes are unlikely. However, the value of L used in [1] (two wavelengths at 20 GHz) may result in box modes being an influence in the L and $2L$ length standards. In addition, the size of the box used in the Sonnet analysis (four wavelengths on a side at 20 GHz) allows 23 box resonances between 3.4–20 GHz for the completely shielded circuit. Thus, we suggest that the small, but noise-like differences are most likely due to box resonances. These box resonances will also exist if the circuit is fabricated as analyzed.

Removal of the box cover, which was done for the Sonnet analyses in [1], changes at least some of the resonances into radiated modes and lowers the Q of other resonances. The complete removal of the box sidewalls (as in unshielded analysis) changes all of the lossless box resonances into lossy radiated waves (the discrete eigenmode spectrum becomes continuous). The basic problem still exists in both cases, with its form depending only on whether an analysis is shielded or unshielded.

For shielded analysis, the differences tend to be noise-like with frequency due to the discrete nature of box resonances. This noise-like behavior is also seen when such circuits are fabricated and is generally considered to be a design failure, not an analysis failure. For a completely shielded circuit, a high-resolution frequency sweep typically resolves the noise into discrete box resonances.

For unshielded analysis, the data tend to be smooth, but lossy. An advantage of the shielded analysis is that, when the box resonance failure mode is excited, it is easily seen in the resulting noisy data. For unshielded analysis, additional evaluation is required to verify that radiation modes are significant. This is important, as undetected radiation

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can result in costly design failures. We emphasize that this is a characteristic of unshielded analysis, not of SOC.

This also illustrates why such circuits should be analyzed in the actual environment in which they are to be used, i.e., shielded or unshielded. If unshielded, that environment includes all potentially coupling circuits, sometimes even at considerable distance.

In [2], it is pointed out that the double-delay technique is readily extended to multiple coupled ports by viewing A–D in the $ABCD$ matrices as matrices themselves. This was implemented in Sonnet at the same time as the original double delay and was even used in the VSOC validation presented in [1].

As for the underlying EM analysis, dynamic range is regularly seen to exceed 100 dB, sometimes even exceeding 180 dB [5]. Thus, analysis dynamic range is unlikely to be an issue here.

Application of modern microwave measurement deembedding techniques to EM analysis remains an important research area and the author is pleased to see the valuable contribution to the state-of-the-art represented by [1].

REFERENCES

[1] V. I. Okhmatovski, J. Morsey, and A. C. Cangellaris, "On deembedding of port discontinuities in full-wave CAD models of multiport circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 51, pp. 2355–2365, Dec. 2003.

[2] J. C. Rautio, "A de-embedding algorithm for electromagnetics," *Int. J. Microwave Millimeter-Wave Computer-Aided Eng.*, vol. 1, no. 3, pp. 282–287, July 1991.

[3] ——, "A time–harmonic electromagnetic Analysis of shielded microstrip circuits," Ph.D. dissertation, <DEPT. OF ???,> Syracuse Univ., Syracuse, NY, 1986.

[4] J. C. Rautio and R. F. Harrington, "An electromagnetic time–harmonic analysis of shielded microstrip circuits," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-35, pp. 726–730, Aug. 1987.

[5] J. C. Rautio, "Testing limits of algorithms associated with high frequency planar electromagnetic analysis," in *Eur. Microwave Conf. Dig.*, Munich, Germany, Oct. 2003, pp. 463–466.

Authors' Reply

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The comments by Dr. Rautio touch upon important issues pertinent to the short-open calibration (SOC) technique and the vector short-open calibration (VSOC) method proposed in [1] for the case of multiple coupled ports. Comparative remarks on the performance of SOC versus the double-delay deembedding technique [2] utilized in the Sonnet software [3] appear to be of particular interest. We address them below in the order of their appearance in the comments. We would also like to refer the reader to the discussion in [4]–[8] for further details on the related issues.

In response to the comment that the double-delay approach is closely related to the SOC method, we would like to point out that the two methods differ in how the calibrating standards are driven and how the information from the full-wave simulation is processed. The calibrating standards themselves utilized in double delay and SOC can be interchangeable between the two approaches. To elaborate, we refer to [1, eq. (16)]. From [1, eq. (16)], the port currents IS and reference plane currents IS' from the shorted L-standard [1, Fig. 5(b)] together with port current IO from the open L-standard [1, Fig. 5(b)] suffice to determine the network parameters of the feed networks subjected to deembedding. It is straightforward to see that while currents IS and IS' can be obtained from the $ABCD$-matrix of the double delay's L standard, the double delay's $2L$-standard $ABCD$-matrix can provide port currents IO under antisymmetric excitation. The reverse statement that the currents IS, IS' and IO obtained from the SOC's short and open L-standards can be used to determine the $ABCD$ matrices of the double delay's L- and $2L$-standards holds as well. Thus, it is the difference in the algorithms for processing the voltage and current data that leads to the different capabilities and restrictions imposed of the SOC and double-delay methodologies.

One of the double-delay's main restrictions is that, in its current form, it can be implemented only in conjunction with the shielded electromagnetic analysis. The restriction is imposed by the necessity to connect ports to the conducting walls in order to ensure the shunt topology of the port discontinuities. This prevents application of double delay to modeling of unshielded circuits that exhibit strong radiated emissions since simulation of such circuits in the shielded environment typically leads to an erroneous response due to waves bouncing off the walls and interfering with the circuit.

As pointed out in Dr. Rautio's comments, the shielded environment modeling and shunt discontinuity restriction come along with the prize of robust self-checking ability ($A = D = I$, $B = 0$) for the sidewall port discontinuity $ABCD$-matrix. The advantage of this procedure, however, can be attributed to both double delay and SOC for as long as the wall-backed ports are utilized. It is important to mention that, for other port types, neither double delay, nor SOC can rely on this property and more general deembedding verification procedure needs to be devised. Our preliminary studies suggest that the feed network S-matrices [1, eq. (19)] can be utilized as an alternative to verify the quality of deembedding. Namely, it was observed that, in case of successful deembedding, the power conservation $\sum_{i=1}^{P_n} |S_{i,j}|^2 \cong 1$ holds for each jth port of excitation in [1, (19)]. Here we use the $\cong$ sign because of unaccounted losses due to radiation. The same power balance was found to grossly deviate from the unity when deembedding failure occurs due to, for example, the resonant length of the feed network.

In both SOC and double-delay methodologies, the power leakage into any type of radiation (substrate surface-wave radiation or spatial-wave radiation) has a detrimental impact on the quality of deembedding. Herewith, the general rule applies that accurate extraction of the network parameters for weakly coupled ports cannot be achieved if the level of radiation exceeds or is close to the level of coupling between such ports. The strength of the radiation impact on the deembedding quality can depend on various factors such as frequency of the time–harmonic analysis, length of the calibration standards (feed networks), thickness of the substrate, topology of the circuit, as well as various others. While specific recommendations on the emission reduction are usually case dependent, a general guideline can be devised for both the shielded and unshielded electromagnetic analysis.

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