Electromagnetic Macro-modeling of 3D High Density Trenched Silicon Capacitors for Wafer-Level-Packaging

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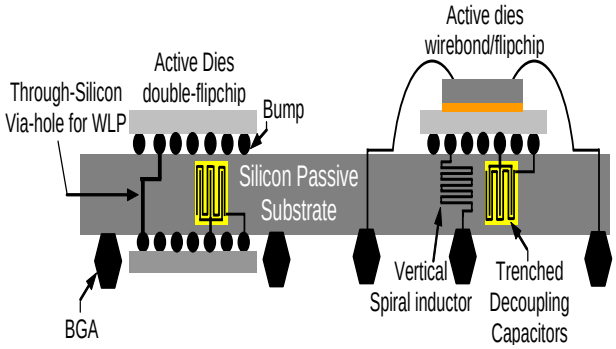
Abstract **— In this paper a full-wave electromagnetic (EM) macro-modeling of 3D high-density trenched capacitors is proposed based on planar EM Method of Moments. The results are used to derive scalable wide-band SPICE-compatible models synthesis easy to include in Physical Design Kit (PDK) libraries for frequency and time domain block-level and system-level simulations. Comparison of both EM macro-models and wide-band extracted models with measurement data for various test case structures demonstrate satisfactory results for frequencies up 50GHz.**

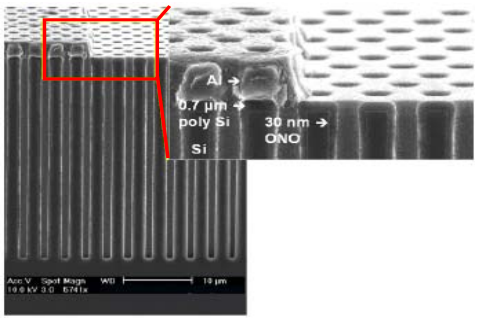
Keywords**—Electromagnetic macro-modeling, Compact wide-band models, model synthesis, 3D high-density trenched capacitors, Wafer-Level Packaging, System-in-Package (SiP), System-on-Chip (SoC).**

I. INTRODUCTION

New mixed-signal integrated circuits, both at component level and function block level, are taking advantage of the third dimension in fabrication technologies, leading to innovative device architectures with improved functionality and performance. At system level, the use of the third dimension for through-Silicon via-hole connections towards full-WLP (Wafer-Level-Packaging) as well as for stacking multi-technology dies in SiP (System-in-Package) applications opens new avenues for reduced design cycles with low cost, smaller feature sizes, lower power consumption [1]. To bring SoC (System-on-Chip) solutions beyond Moore's law, advanced integration solutions for passive devices that used to be outside the chips, are being investigated. Among such emergent techniques, a novel 3D high-density trenched capacitor recently proposed by Philips-NXP-semiconductors for advanced multi-technology integration have demonstrated high performances reaching 25-250nF/mm^2 capacitance with ESR (Estimated Series Resistance) and ESL (Estimated Series Inductance) less than 100mΩ and 25pH, respectively. The trenched capacitors are integrated in macroporous Si-wafers with dielectric layers manufactured using conventional front-end techniques, like CVD and thermal processing, containing over 1 billion macropores. Compared to high k materials made with lower temperature processes subject to defect densities, the proposed technology solution leads to higher quality factors resulting in part from low dielectric losses and piezoelectric relaxation phenomena inside the material. Concurrently advanced technologies such as Silicon chips onto other Silicon chips (double flip-chip) are fully supported by the proposed Silicon technology solutions, based on a combination of most advanced micro-bumping with die placement techniques. The resulting technologies require very challenging methodologies to be properly analyzed using available electromagnetic solutions. The geometric topology of the 3D high-density trenched capacitors exhibit significant ratio dimensions exceeding many hundreds following the third integration direction. Such multi-scale attributes impose very severe meshing complexity on 3D volume meshing methods with unacceptable CPU time and memory requirements even when advanced adaptive meshing algorithms are considered.



(a)



(b)

Fig.1 Silicon-based System Level Integration taking advantage of third dimension integration (e.g., high density trenched capacitors, vertical spiral inductors) (a), Photograph of the 3D high-density trenched capacitor (b).

This paper discusses an electromagnetic macro-modeling approach for efficient analysis of integrated components that take advantage of the third dimension degree of freedom. The proposed approach is successfully applied to the characterization and modeling of 3D high density trenched capacitors for frequencies up to 50GHz. The resulting electromagnetic results are used to derive scalable wide-band SPICE-compatible models [2] easy to include in PDK libraries for frequency and time domain block-level and system level simulations. Comparisons of extracted models with measurement data for various test case structures show very satisfactory results.

II. Description of the Macro-Modeling Methodology for 3D High Density Silicon Trenched Capacitors and Definition of Test Case Structures

The proposed methodology compresses the physical attributes of the 3D high-density trenched capacitors into an equivalent macro-model with reduced complexity leading to similar /equivalent electrical behavior. A space-mapping approach applied to the dielectric parameters (permittivity and thickness) to align the resulting macro-model in regards to nF/mm with the original dedicated test case structures. The number of trenched macroporous holes are represented by nested electrodes using planar assumptions as shown in Fig.2a, and b. Dedicated test-case structures characterize different 3D high-density trenched capacitors through Ground-Signal-Ground (G-S-G) probing measurement (in Fig.2(c)).

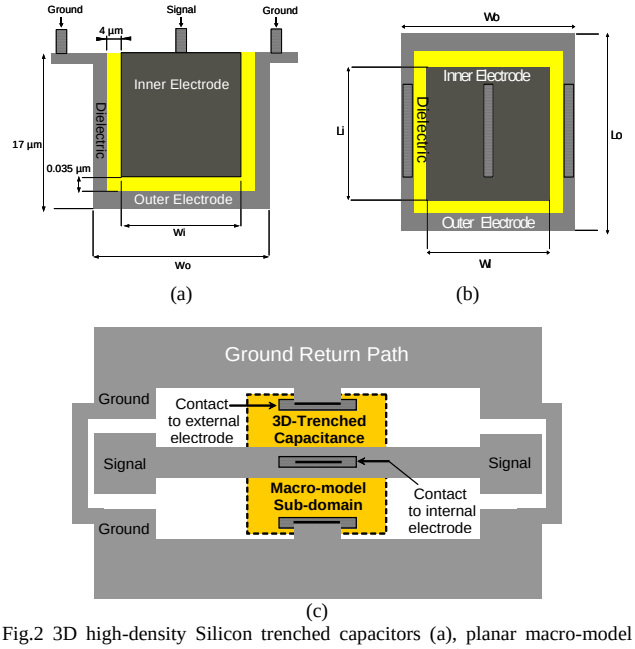


Fig.2 3D high-density Silicon trenched capacitors (a), planar macro-model cross-section side view, (b) top view, and (c) top view of entire test structure.

The designed/measured probing patterns are included in the simulated electromagnetic macro-model including via-hole inter-metal connections contacting the capacitance electrodes to properly synthesize the frequency dependent ESR and ESL contributions required for accurate estimation of quality factors and resonant frequenecies. The pattern of the 3D high-density Capacitor shown in Fig.1 is based on a shunt capacitance configuration to minimize impact of parasitic effects resulting from the feeding lines and ground return path.

III. Discussion of the Results and Validation

A. *Electromagnetic Macro-model Smulation: Comparison with Measurement*

On-wafer measurements are performed on various 3D high-density capacitor structures using a Network Analyzer (E8364B_HP4141) and coplanar G-S-G probes in the frequency band 0.1-50 GHz, assuming shunt configurations. In addition to shunt configuration, different connection options are considered so as to synthesize high-density capacitor values based on parallel combination of elementary cells to reduce series parasitic effects resulting from resistance and inductance.

The high-density trenched capacitor structures are fabricated using customized NXP-Philips Semiconductors low cost, high resistivity silicon PICS (*Passive Integration Connecting Substrate*) technology. A simplified two-metal layer cross-section of the substrate stack is composed of a 650 µm thick silicon substrate with a conductivity of 0.1 S/m (equivalent to a resistivity of 1000 Ωcm) covered by a 0.50 µm thick insulationg SiO_2 layer. The two-metal layers (Fig. 3) are used to contact the internal and external electrodes of the trenched capacitors composed of poly-silicon (PS layer) and low resistivity material (HL layer), with a 0.035µm thick dielectric in between. The parameters of the dielectric in the electromagnetic macro-model, Fig. 2, are adjusted to match the capacitance of the test structure, Fig. 3. . The electromagnetic macro-model effectively compresses the 3D capacitance into a planar description that conserves the geometric topology (Li, Wi, Lo, Wo in Fig2b) and normalized capacitance per unit area of the measured device. Fig.4a and b show comparison of different electromagnetic macro-models (*option 1=coarse representation and option 2=fine representation*) with measurement for S_{11} and S_{12} (in dB) parameters demonstrating satisfactory correlations.

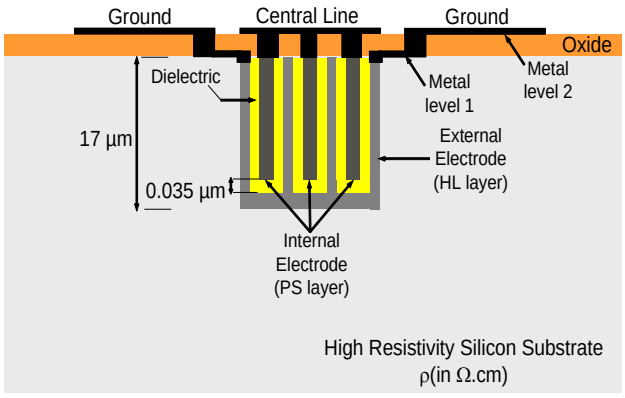


Fig.3 PICS (Passive Integration Connecting Substrate) technology Cross-section.

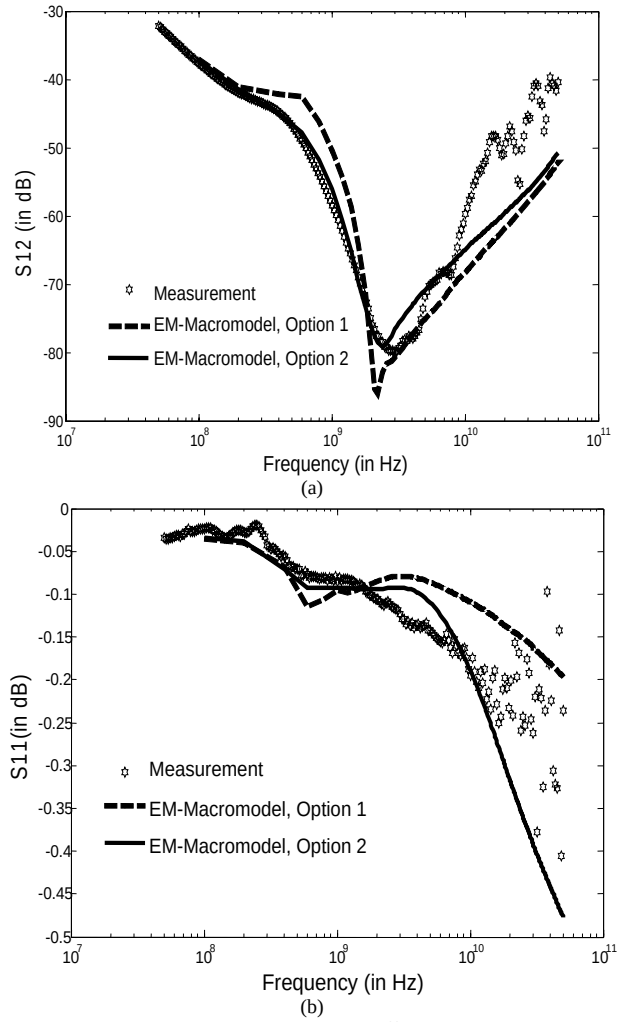


Fig.4 Comparison between Measurement and different EM simulation macro-models (Coarse and Fine) for S12 (a), and S11 (b) against frequency.

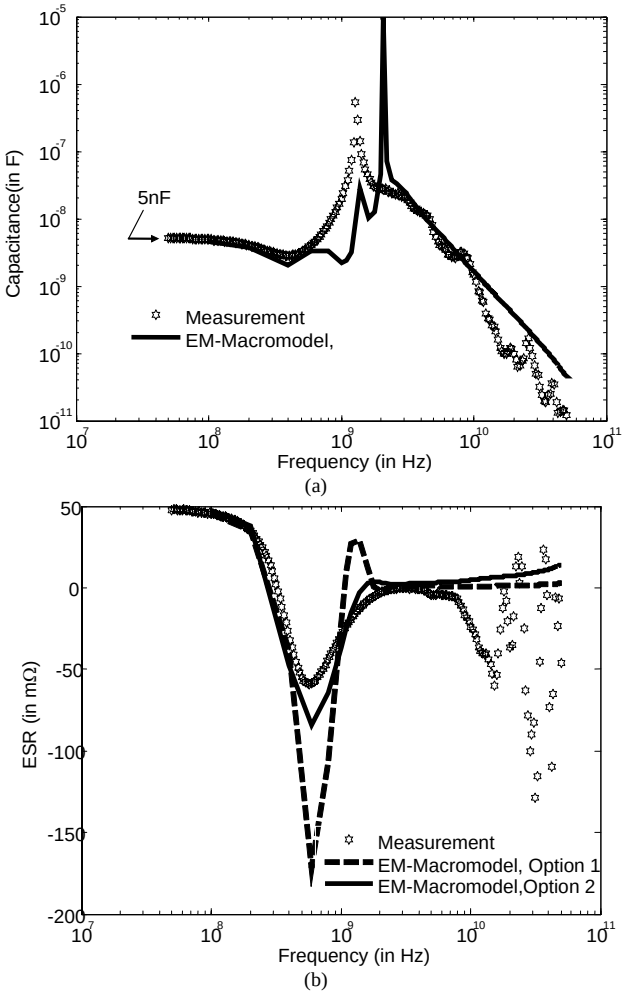


Fig.5 Extracted Shunt Capacitance (a) and ESR (Estimated Serial Resistance) (b) from measurement and from EM macro-model.

In Fig.5(a) and Fig.5(b) extracted shunt capacitance $Cshunt=1/[\omega Imag(Z_{12})]$ and the estimated serial resistance $ESRshunt=Real(Z_{12})$ are extraction from the trans-impedance parameter Z_{12} assuming a T-equivalent circuit topology following the pattern of the 3D trench Capacitance shown in Fig.2 and Fig.3 based in shunt configuration. ESR values of 47mΩ, 47.4mΩ and 45.4 Ω are extracted respectively from the measurement and from electromagnetic macro-model simulations (option 1 and option 2 respectively) at 0.1 GHz. Negative values of extracted ESR in Fig. 5 at high frequency result from single T-model topology not accounting for distributed effects.

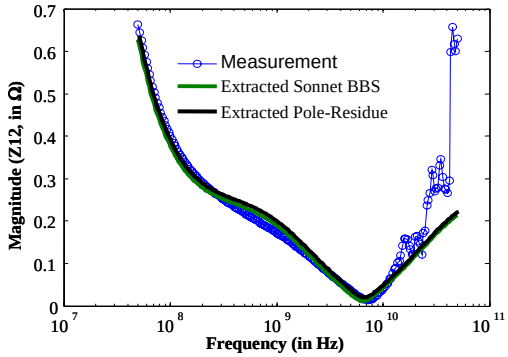
Extracted capacitance of 4.89nF is obtained from the measurement data. Low frequency quasi-static close-form approximations using parallel plate equivalent area of 265µm by 242µm assuming inter-electrode dielectric layer thickness of 0.035µm lead to 5.032nF (neglecting fringing effects) and 5.032nF (including fringing effects, [3]).

B. Compact Broadband Circuit Synthesis

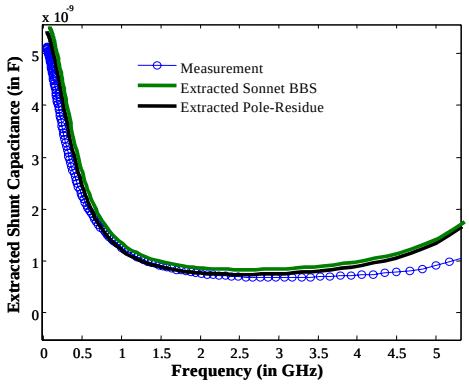
Single-T model extractions in Fig.5 show strong dependence of shunt capacitance and ESR parameters against frequency. From such narrow band assumptions, the shunt capacitance and ESR parameters become negative at high frequencies demonstrating necessity for the trench capacitors to account for distributed effects through efficient wideband synthesis. Synthesis from EM results or measurement data of SPICE-compatible compact equivalent circuit models allows for coupled time/frequency domain analysis in combination with transistor level description of active components/sub-modules. To synthesize wide-band equivalent models from the electromagnetic macro-models or measurement for the simulated high-density trench capacitors different approaches are investigated and compared. The first approach uses Sonnet BBS (Broad-Band SPICE) extraction tool based on a black-box representation. The second approach is based on a manual extraction procedure using pole-residue expansions to cast the impedance/admittance parameters in a pole-residue form. The

resulting transfer functions are synthesized with frequency-independent R, L, and C elements.

Fig.6(a),(b) depicts comparisons between Sonnet-BBS synthesis, manual pole-residue expansion method and measurement results for the trans-impedance parameter (in magnitude) and extracted shunt capacitance against frequency, showing satisfactory agreement.



(a)



(b)

Fig.6 Comparison between Sonnet BBS extraction, wideband equivalent circuit model extracted using manual pole-residue and measurement data for the magnitude of trans-impedance parameter Z_{12} and extracted shunt capacitance versus frequency.

The wide-band compact model resulting from the pole-residue expansion approach is represented in Fig.7. While the aforementioned two extraction approaches lead to reasonable accuracy, they bring some limitations. The BBS approach remains mathematically abstract as it is a black-box representation with no interpretation in terms of the physical component being modeled. It should be emphasized that manual extractions based on pole-residue expansion method is expensive to implement since selection of topology branches given a set of pole and residue terms is not straightforward. In addition, non-physical elements can be extracted with the pole-residue expansion approach (negative resistance, capacitance, or inductance) leading to passivity/stability preservation issues [4-6]. A newly developed compact lumped models synthesis methodology presented in [2] can be used for an automatic synthesis of a compact model for a portion of the considered capacitors.

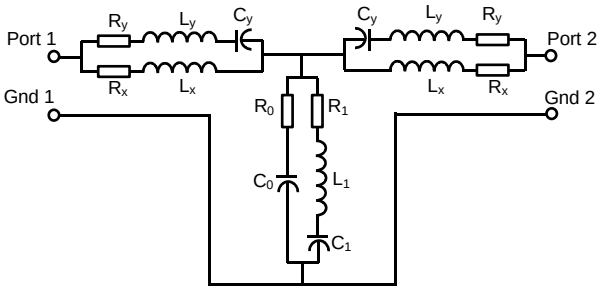


Fig.7 Wideband equivalent circuit model extracted using manual pole-residue expansion synthesis with L_y=0.1nH, R_y=76.6Ω, R_x=0.044Ω and L_x=0.074nH, C_0=5nH, R_0=0.267Ω, R_1=0.011Ω, C_1=5nF,L_1=0.0012nH.

IV. Conclusion

A full-wave electromagnetic macro-modeling methodology of 3D high-density trenched capacitors has been proposed based on planar assumptions. The proposed methodology properly captures the distributed nature of the trenched capacitors which is not easy to represent with lumped elements assumptions. Comparisons of electromagnetic macro-model results with on-wafer measurement data for various test case structures show satisfactory agreement with accurate estimates of low-frequency ESR and shunt capacitance values. Systematic synthesis of compact wideband equivalent circuit models scalable with respect to device topology and electrical performances is being investigated. The proposed macro-modeling approach in combination with through-wafer via-hole connections make possible Wafer-Level-Packaging (WLP) simulation and analysis.

Acknowledgment

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References

[1] Rao R. Tummala, ‘‘SOP: What Is It and Why? A New Microsystem-Integration Technology Paradigm-Moore’s Law for System Integration of Miniaturized Convergent Systems of the Next Decade’’, ”, IEEE Transactions on Advanced Packaging, VOL. 27, NO.2, pp.241-247,Feb. 2004.

[2] J.Rautio, Synthesis of Compact Lumped Models from Electromagnetic Analysis Results, *IEEE Trans. Microwave Theory Tech.*, accepted for future publication.

[3] Thomas H. Lee, The Design of CMOS Radio Frequency Integrated Circuits, Cambridge University Press 1998, page 38.

[4] B. Gustavsen and A. Semlyen, “Enforcing passivity for admittance matrices approximated by rational functions,” *IEEE Trans. Power Syst.*,vol. 16, no. 1, pp. 97–104, Feb. 2001

[5] D. Saraswat, R. Achar, and M. S. Nakhla, “A fast algorithm and practical considerations for passive macromodeling of measured/simulated data,” *IEEE Trans. Adv. Packag.*, vol. 27, no. 1, pp. 57–70, Feb. 2004.

[6] S. Grivet-Talocia, “Passivity enforcement via perturbation of Hamiltonian matrices,” *IEEE Trans. Circuits Syst.—I*, vol. 51, no. 9, pp.1755–1769, Sep. 2004.